JOURNAL OF MATERIALS SCIENCE 27 (1992) 5531–5535

Growth and characterization of Al_2O_3 insulator gate on p-InP and p-Si by metallorganic chemical vapour deposition at low temperatures

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Metallorganic chemical vapour deposition of Al_2O_3 from $Al(O-C_3H_7)_3$ via pyrolysis at low (~ 280 °C) temperature was investigated with the goal of producing high quality Al_2O_3/p-InP (1 0 0) and Al_2O_3/p-Si (1 0 0) interfaces. Ellipsometer measurements of Al_2O_3 have determined the refractive index of the film to be about 1.55. Room temperature capacitance-voltage measurements were used to characterize the electrical properties of the structures after metal gate electrodes have been deposited. Low temperature conductance-voltage measurements were also carried out to investigate the quality of the Al_2O_3/InP interfaces. The interface state densities Al_2O_3/p-InP and Al_2O_3/p-Si determined from deep-level transient spectroscopy were approximately 10^{12} eV^{-1} cm^{-2} and 10^{11} eV^{-1} cm^{-2}.

1. Introduction

Rapid advances in growth technology of metallorganic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE) have made possible the fabrication of several new types of metal–insulator–semiconductor (MIS) systems with III–V compound semiconductor substrates [1]. The application of GaAs–MIS capacitors using several kinds of insulators has not been very successful so far due to the pinning of the Fermi level near midgap which is caused by a huge density of interface states [2]. However, InP–MIS capacitors are particularly interesting due to their applications in high-speed digital circuits and high-frequency power amplification [3–5]. Furthermore, since the Fermi level in the case of the MIS capacitors can be moved nearly across the whole bandgap, both inversion and accumulation can be achieved [6].

Many groups have investigated SiO_2 [7–9] and Si_3N_4 [10, 11] as possible deposited insulators for InP–MIS applications. However, since the deposition temperature must be kept below the InP decomposition temperature [12], in this study, for the fabrication of insulator gates, Al_2O_3 was deposited on p-type InP (100) and Si (100) by MOCVD at about 280 °C [1, 13, 14]. Also, since much information is already available about insulator/Si interface structures [15], Al_2O_3 was also deposited on p-Si (100) substrates. There is currently much interest in heteroepitaxial Al_2O_3 films on Si (100) by low pressure chemical vapour deposition (LPCVD) [16] and metallorganic molecular beam epitaxy (MOMBE) [17] due to the long-range goal of three-dimensional integrated circuits, and in epitaxial thin films of $YBa_2Cu_3O_7$ grown successfully on $Al_2O_3\{1 0 1 2\}$ by a laser ablation technique [18].

To remove the native oxide layer prior to deposition of the Al_2O_3 gate insulator, the HCl vapour etching technique [18, 19] was employed at 200 °C for 2 min. Ellipsometer measurements were carried out to determine the refractive index of the Al_2O_3, and room temperature capacitance–voltage (C–V) and low temperature conductance–voltage (σ–V) measurements were performed to investigate electrical properties for InP–MIS and Si–MIS. Also, deep-level transient spectroscopy (DLTS) measurements were used to determine interface state densities at Al_2O_3/InP and Al_2O_3/Si structures.

2. Experimental procedure

The carrier concentrations of p-InP and p-Si substrates with (1 0 0) orientation used in this experiment are 1×10^{14} cm^{-3} and 1×10^{-15} cm^{-3}, respectively. After InP substrates were alternately degreased in warm acetone and trichloroethylene three times, they

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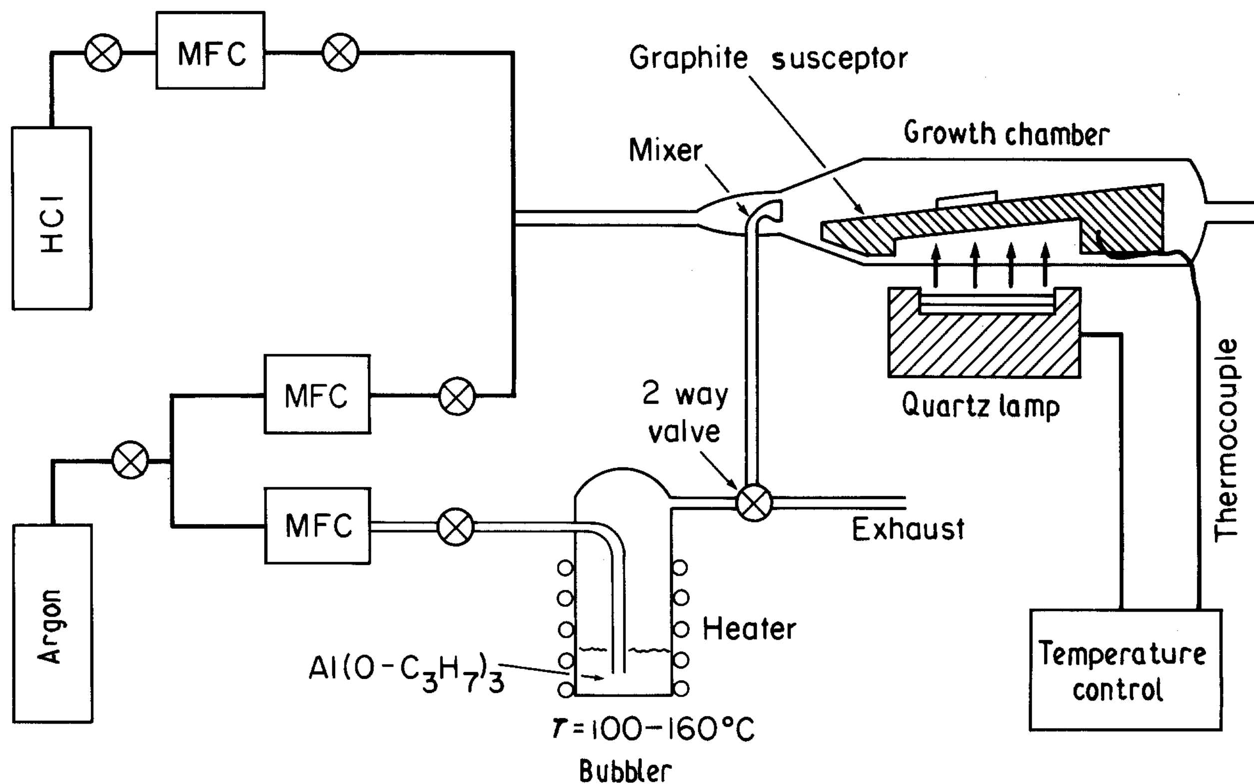


Figure 1 Schematic diagram for the *in situ* HCl vapour etching and Al_2O_3 deposition.

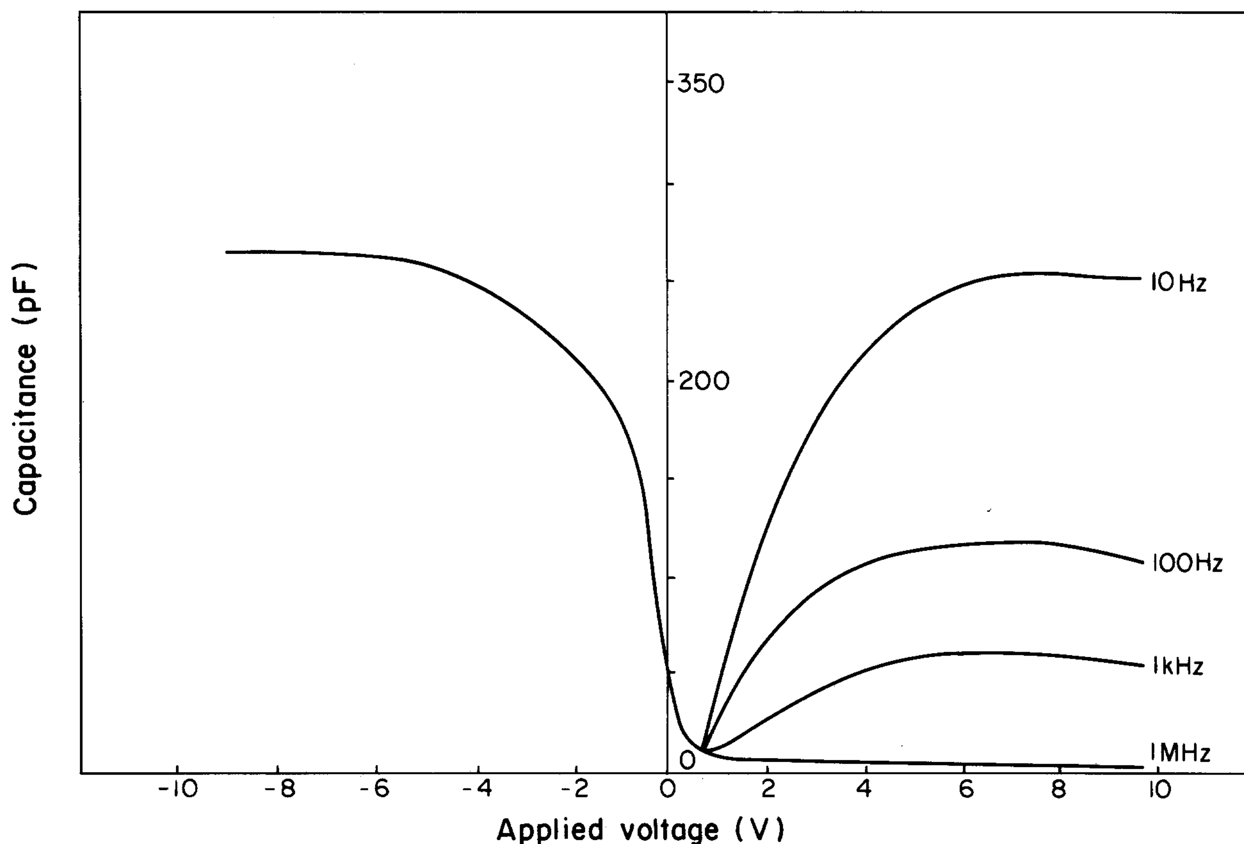
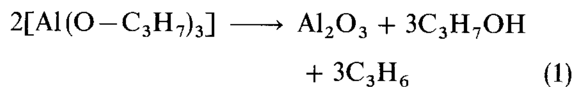


Figure 2 Capacitance–voltage curves dependent on various frequencies of $Al/Al_2O_3/Si$–MIS capacitor. Sweep rate = $10\,mV\,s^{-1}$.

were etched in Br–methanol solution mechanochemically, rinsed in deionized water thoroughly, and etched in a mixture of H_2SO_2, H_2O_2 and H_2O (4:1:1) at 40 °C for 10 min. As soon as the etching process was finished, the wafer was put on a graphite heater in the MOCVD chamber, and the chamber was evacuated to 1.333×10^{-1} Pascal by a mechanical pump. The useful vapour etching methods for the InP involve the HCl reaction techniques which are used in vapour phase epitaxial growth technology for III–V compound

semiconductors. In this case, the reaction chamber can be used for not only the HCl vapour etching, but also for Al_2O_3 insulator deposition. The schematic diagram is shown in Fig. 1.

Prior to the HCl vapour etching, the residual gas inside the chamber was purged with pure Ar gas for approximately 1 h. The HCl vapour etching was carried out in an Ar atmosphere containing pure HCl gas with a flow rate of about 200 ml min^{-1} at 200 °C for 2 min. The etch rate of the HCl vapour etching on InP (1 0 0) substrate carried out at 200 °C was estimated as 5×10^4 nm min^{-1}. After the HCl vapour etching was completed, pure Ar gas removed the surrounding HCl vapour inside the chamber for 30 min, and the Al_2O_3 gate insulator was deposited on the polished InP substrates in the same chamber with an Ar flow rate of about 50 ml min^{-1} at 250–300 °C. Also, for comparison with a well known Si-MIS, the Al_2O_3 gate insulator was also deposited on the clean p-Si substrates using similar methods. In this process, Al $(O-C_3H_7)_3$ was decomposed into Al_2O_3, C_3H_7OH and C_3H_6. The C_3H_7OH and C_3H_6 were removed with Ar gas, while the Al_2O_3 was deposited on the substrates. The chemical reaction by pyrolysis in the procedure is given by the following equation:



$$2[Al(O-C_3H_7)_3] \longrightarrow Al_2O_3 + 3C_3H_7OH + 3C_3H_6 \quad (1)$$

Device processing involved fabrication of an array of Al metal gates on the Al_2O_3 surface and Au–Zn ohmic contact to the bulk p-type InP substrates for the *C–V* measurements dependent on various frequencies. Variable-frequency *C–V* and DLTS measurements were performed by operating the 1 MHz capacitance meter in conjunction with a lock-in amplifier and a pulse generator. Capacitively coupled conductance–voltage (σ–V) measurements at 4.2 K were also carried out.

In order to investigate the possibility of the MIS capacitor using the Al_2O_3 layer as a gate insulator, $Al/Al_2O_3/Si$–MIS grown with an Ar gas flow rate of about 60 ml min^{-1} at 280 °C for 12 min was characterized by *C–V* measurements dependent on various frequencies as shown in Fig. 2. This behaviour is almost similar to the *C–V* measurements of $Al/Al_2O_3/Si$ at substrate temperatures above 1000 °C grown by low-pressure chemical vapour deposition (LPCVD) with the use of $Al(CH_3)_3$ and N_2O as reported by Ishida *et al.* [16] and that of ordinary $Al/SiO_2/Si$ [20]. The thickness of the Al_2O_3 gate insulator determined by *C–V* measurements is about 6×10^4 nm, and this value is considered to be in reasonable agreement with the magnitude which was measured by the ellipsometer.

In conjunction with Si–MIS capacitors, 1 MHz *C–V* profiling at room temperature was carried out on similar InP (1 0 0)–MIS structures as shown in Fig. 3. Among many samples grown under different conditions, the Al_2O_3 gate insulator of this sample was grown at an Ar gas flow rate of about 50 ml min^{-1} at 280 °C for 10 min. From the maximum accumulation capacitance of a single *C–V* curve, the thickness of Al_2O_3 was determined to be approximately 1.2×10^4 nm. The colour of the Al_2O_3 gate insulator was pale blue. Since the expected colour of the Al_2O_3 has an immediate connection with refractive index and film thickness, the refractive index of the Al_2O_3 was determined by the ellipsometer. Ellipsometer measurements have shown it to be about 1.55.

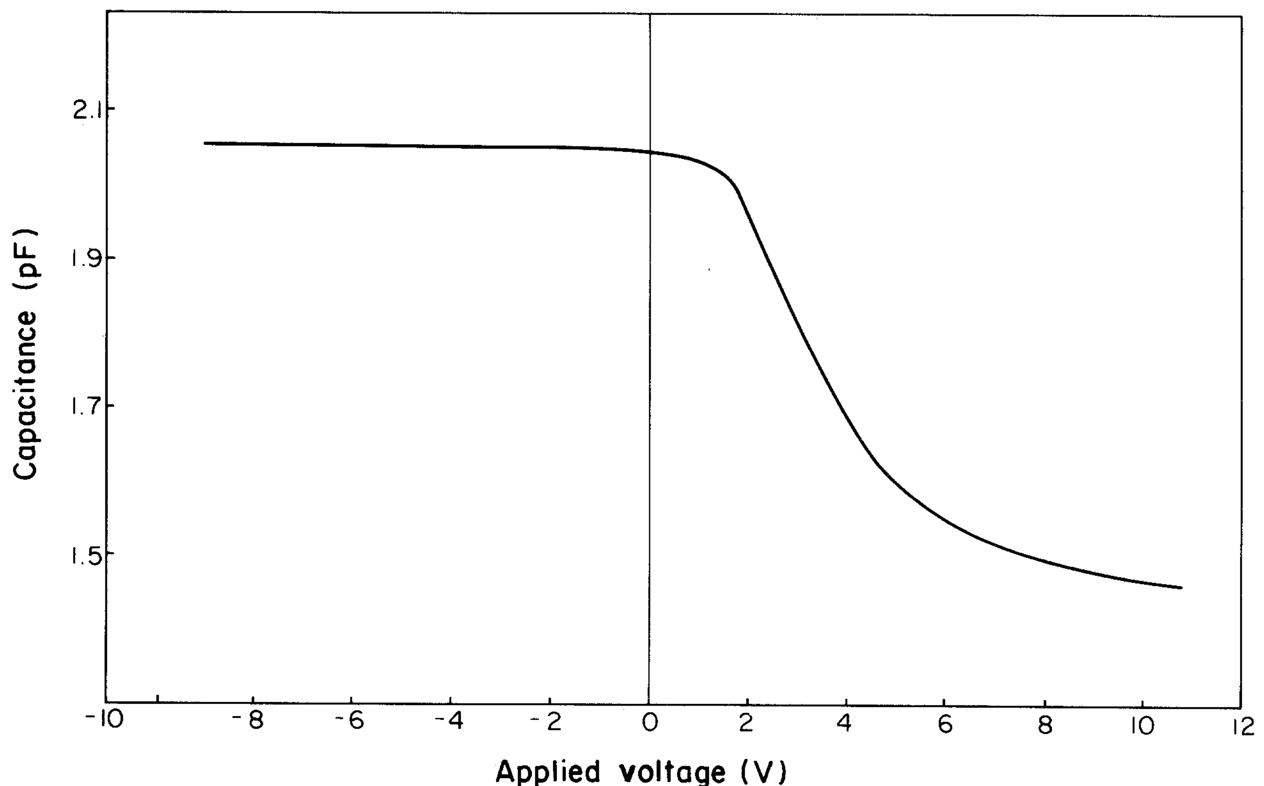


Figure 3 1 MHz $Al/Al_2O_3/InP$–MIS capacitance–voltage curve. Sweep rate = 10 mV s^{-1}.

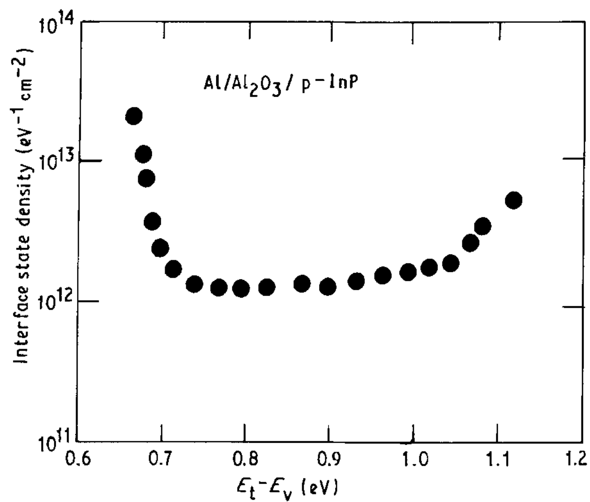


Figure 4 Interface state densities of the $Al/Al_2O_3/InP$–MIS system as a function of energy, obtained from DLTS measurements.

However, because insulator/semiconductor interface qualities can be changed according to the growth methods and various kinds of insulators, the interface state densities of Al_2O_3/InP and Al_2O_3/Si structures were investigated by DLTS measurements. The interface state densities of Al_2O_3/InP were determined from DLTS measurements as shown in Fig. 4. The interface state density has been found to be approximately $10^{12}\ eV^{-1}\ cm^{-2}$ at the middle of the energy gap. These values are comparable with those obtained from $Al/SiO_2/InP$ capacitors by Staa *et al.* [6] and Bogdanski *et al.* [21] in the energy range of about 0.7–1.0 eV. This may be caused by carbon contamination at the Al_2O_3/InP interface or the Al_2O_3 insulator gates. Detailed studies on the Al_2O_3/InP interface will be presented in another publication. Also, the distribution shapes of the interface state density at the Al_2O_3/Si structure determined from DLTS were similar to those at the Al_2O_3/InP structure, and it had an interface state density of approximately $10^{11}\ eV^{-1}\ cm^{-2}$ at the middle of the energy gap. Although this magnitude is somewhat higher than that of the high quality SiO_2/Si structure, the value of the Al_2O_3/Si interface state density is sufficiently low for application in three-dimensional integrated circuits and MIS devices [16, 22].

In addition to C–V measurements at room temperature, capacitively coupled C–V measurements were carried out to investigate the existence of impurities at the Al_2O_3/InP interfaces. The fundamental idea of this method is to couple capacitively to the conduction layer through an Al_2O_3 layer by applying a megaHertz-range radiofrequency voltage to the pair of capacitive contacts on a chromium resistive gate [23]. The capacitive contacts of highly conducting aluminium of $\sim 1\ \mu m$ thickness are evaporated on the top surface of the resistive metal chromium gate layer of $\sim 1 \times 10^3$ nm thickness. Backside contacts to the substrate of p-type InP were fabricated by Au–Zn diffusion at 450 °C in a H_2 atmosphere for approximately 10 min. The results of measurements on $Al/Cr/Al_2O_3$/p-InP at 4.2 K are shown in Fig. 5. Even if such measurements at low temperature were not supposed to show any conductance as a result of the freezing-out of acceptors in the p-type bulk InP substrate, conductance varied depending on the applied gate voltage as shown in Fig. 5. However, it is impossible to determine unambiguously from the σ–V measurements whether the origin of the carriers which contribute to some magnitude of conductivity is due

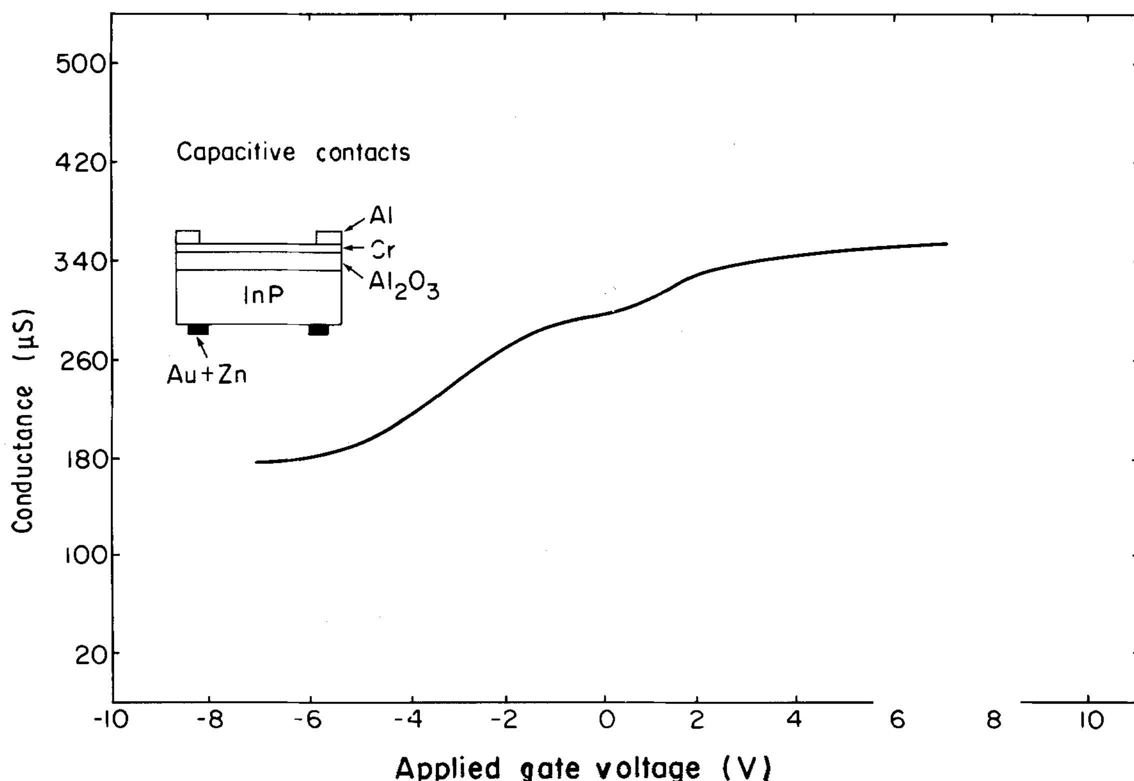


Figure 5 Conductance–voltage measurements on $Al/Cr/Al_2O_3/InP$ at 4.2 K.

to the damage layer on the surface of the InP bulks, and is itself the source of conductivity, or whether a band of donor-like surface defects at energy above the conduction band edge cause conductivity variation of the p-type InP at Al_2O_3/InP interfaces.

3. Summary and conclusion

The present results of $C-V$ measurements at room temperature demonstrate clearly MIS behaviours for MOCVD samples with the Al_2O_3 gate insulator grown directly on HCl vapour-etched p-Si and p-InP substrates via pyrolysis at 280–300 °C from $Al(O-C_3H_7)_3$. The thickness of Al_2O_3 can be regulated by Ar flow rate and growth time to be in the range 10^4–7×10^4 nm. Ellipsometer measurements indicated that the refractive index was 1.55. The interface state density at the Al_2O_3/InP structure determined from DLTS has been found to be approximately $10^{12}\ eV^{-1}\ cm^{-2}$ in the energy range between about 0.7 and 1.0 eV, and that at the Al_2O_3/Si structure has been observed to be about $10^{11}\ eV^{-1}\ cm^{-2}$ at the middle of the energy gap. Conductance–voltage measurements with capacitive contacts and a resistive gate show increasing conductivity of the channel with positive gate voltages. Although some details remain to be clarified, these observations possibly have interesting device implication. With a p-type or low density n-type InP buffer layer it should be possible to produce InP–MIS capacitors and InP–MISFET with high quality Al_2O_3/InP interfaces. Furthermore, Al_2O_3 insulator gates grown at low temperatures give good motivation for fabrication of InSb–MIS diodes and InSb–MISFET, and high quality Al_2O_3 epitaxial films hold promise for buffer layers for the growth of epitaxial $YBa_2Cu_3O_7$ thin films.

Acknowledgements

The work at Kwangwoon University was supported in part by the Korean Ministry of Education, and the work at SUNY-Buffalo was supported in part by the office of Naval Research.

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Received 24 June
and accepted 27 November 1991